LISTING OF THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in this application.

Claim 1-8 (Canceled)

Claim 9 (Original): A method of designing a semiconductor device, comprising:

a step of measuring a thickness of a pad oxide film formed on a surface of a semiconductor substrate and a thickness of a nitride film formed on said pad oxide film;

a step of measuring an internal stress of said nitride film;

a step of measuring the width of a device formation region formed on said semiconductor substrate and a width of a device isolation region adjacent to said device formation region;

a step of measuring a depth of a groove formed inside said semiconductor substrate by etching a portion existing on said device isolation region among a nitride film formed on said oxide film;

a step of conducting stress analysis using said thickness, said width, said depth and said internal stress and obtaining an internal stress estimated to occur due to thermal oxidation in the proximity of said groove;

a step of preparing a design chart representing a region in which a quotient obtained by dividing said stress by a dislocation occurrence limit stress, at which dislocation occurs due to thermal oxidation, exceeds 1, by using the width of said device formation region and the width of said device isolation region as parameters; and

a step of setting a value of the width of said device formation region and a value of the width of said device isolation region, at which dislocation does not occur, in design of said semiconductor substrate.

Claim 10 (Original): A method of designing a semiconductor device according to claim 9, wherein said groove has a thermal oxidation film formed by thermal oxidation, and which further includes:

a step of applying data of said design chart so as to establish the following formula relating to a dislocation occurrence limit stress value due to thermal oxidation in said device formation region and said device isolation region adjacent to one another:

$$\sigma/\sigma_c = [\{0.78 + 0.054D - 0.00086D^2\} + \{-0.040t_p + 0.00086t_p^2\} + \{0.01t_n + 0.000051t_n^2\}] \times [0.043 + 0.61L - 0.14L^2 + 0.015L^3] \times [1.4 - 0.49S + 0.18S^2 - 0.021S^3] \leq 1$$

wherein L/S in a value of said ratio, t_p is the thickness of said pad oxide film, t_n is the thickness of said nitride film and D is the depth of said groove.

Claim 11 (Original): A method of designing a semiconductor device according to claim 9, which further includes:

a step of deciding an etch-back distance of said pad oxide film not causing the occurrence of dislocation by using said design chart; and

a step of etching and removing said pad oxide film by said etch-back distance in a direction parallel to the surface of said semiconductor substrate.

Claim 12 (Original): A method of designing a semiconductor device comprising:

a step of measuring a thickness of a pad oxide film formed on a surface of a semiconductor substrate, and a thickness of a nitride film formed on said pad oxide film;

a step of measuring an internal stress of said nitride film;

a step of measuring a width of a device formation region formed on said semiconductor substrate, and a width of a device isolation region adjacent to said device formation region;

a step of measuring a depth of a groove formed in said semiconductor device by etching a portion of said nitride film formed on said pad oxide film and existing on said device isolation region;

a step of conducting stress analysis by using said thickness, said width, said depth and said internal stress, and obtaining an internal stress estimated to occur due to thermal oxidation in the proximity of said groove;

a step of preparing a stress distribution chart representing a region, in which said stress exceeds a dislocation occurrence limit stress at which dislocation occurs due to thermal oxidation, by using the width of said device formation region and the width of said device isolation region as parameters; and

a step of setting the width of said device formation region and the width of said device isolation region not causing dislocation by using said stress distribution chart in designing said semiconductor substrate.

Claim 13 (Canceled)

Claim 14 (New): A semiconductor device including:

a semiconductor substrate;

a plurality of circuit forming regions provided at a main surface of said semiconductor substrate, respectively; and

device isolation regions provided as grooves, at least one of said grooves having a depth, extending inwardly from said main surface, greater than 6 nm and a thermal oxide film formed in said groove for isolating said circuit forming regions from one another, each device isolation region having a width taken from the range of values of 0.1 to 2.5 μm,

wherein a width of each of the circuit forming regions is set such that a ratio of the width of each occurrence of a circuit forming region to the width of an adjacent device isolation region having a depth greater than 6 nm is at least 2 and not greater than 50 to prevent stress in the substrate from exceeding a dislocation occurrence limit stress value which is otherwise likely to occur, based on the depth of the grooves exceeding 6 nm, to cause a dislocation at portions of the main surface of the substrate located adjacent mask ends of a mask used to form the grooves.

Claim 15 (New): A semiconductor device according to claim 14,

wherein said circuit forming regions consist of memory circuit regions and peripheral circuit regions,

wherein said device isolation regions include ones for isolating the respective peripheral circuit regions from each other and isolating the respective memory circuit regions from each other, and

wherein said ratio is inclusive of relative widths associated with said peripheral circuit regions and ones of said device isolation regions adjacent thereto, respectively, which have depths of greater than 6 nm and smaller than 50 nm.

Claim 16 (New): In a semiconductor device in which different circuit forming regions are electrically isolated from each other via isolation regions in the form of thermal oxide film formations, the improvement comprising:

a plurality of circuit forming regions provided at a main surface of a semiconductor substrate, respectively; and

device isolation regions provided as grooves, at least one of said grooves having a depth, extending inwardly from said main surface, greater than 6 nm and a thermal oxide film formed in said groove for isolating said circuit forming regions from one another, each device isolation region having a width taken from the range of values of 0.1 to 2.5 μm,

wherein a width of each of the circuit forming regions is set such that a ratio of the width of each occurrence of a circuit forming region to the width of an adjacent device isolation region having a depth greater than 6 nm is at least 2 and not greater than 50 to prevent stress in the substrate from exceeding a dislocation occurrence limit stress value which is otherwise likely to occur, based on the depth of the grooves exceeding 6 nm, to cause a dislocation at portions of the main surface of the substrate located adjacent mask ends of a mask used to form the grooves.

Claim 17 (New): A semiconductor device according to claim 16,

wherein said circuit forming regions consist of memory circuit regions and peripheral circuit regions,

wherein said device isolation regions include ones for isolating the respective peripheral circuit regions from each other and isolating the respective memory circuit regions from each other, and

wherein said ratio is inclusive of relative widths associated with said peripheral circuit regions and ones of said device isolation regions adjacent thereto, respectively, which have depths of greater than 6 nm and smaller than 50 nm.

Claim 18 (New): A semiconductor device including:

a semiconductor substrate;

a plurality of circuit forming regions provided at a main surface of said semiconductor substrate, respectively;

device isolation regions provided as grooves, at least one of said grooves having a depth, extending inwardly from said main surface, greater than 6 nm and a thermal oxide film formed in said groove for isolating said circuit forming regions from one another, each device isolation region having a width taken from the range of values of 0.1 to 2.5 μm; and

means for preventing stress at portions of the main surface of the substrate located adjacent mask ends of a mask used to form the grooves from exceeding a dislocation occurrence limit stress value which is otherwise likely to occur, based on the depth of the grooves exceeding 6 nm, to cause dislocation at said portions of the main surface of the substrate by setting a ratio of the width of a circuit forming region to a width of an adjacent device isolation region within a predetermined range.

Claim 19 (New): In a semiconductor device in which different circuit forming regions are electrically isolated from each other via isolation regions in the form of thermal oxide film formations, the improvement comprising:

a plurality of circuit forming regions provided at a main surface of a semiconductor substrate, respectively;

device isolation regions provided as grooves, at least one of said grooves having a depth, extending inwardly from said main surface, greater than 6 nm and a thermal oxide film formed in said groove for isolating said circuit forming regions from one another, each device isolation region having a width taken from the range of values of 0.1 to 2.5 μm; and

means for preventing stress at portions of the main surface of the substrate located adjacent mask ends of a mask used to form the grooves from exceeding a dislocation occurrence limit stress value which is otherwise likely to occur, based on the depth of the grooves exceeding 6 nm, to cause dislocation at said portions of the main surface of the substrate by setting a ratio of the width of a circuit forming region to a width of an adjacent device isolation region within a predetermined range

Claim 20 (New): A semiconductor device including:

a semiconductor substrate;

a plurality of circuit forming regions provided at a main surface of said semiconductor substrate, respectively; and

device isolation regions provided as grooves, at least one of said grooves having a depth, extending inwardly from said main surface, greater than 6 nm and a thermal

oxide film formed in said groove for isolating said circuit forming regions from one another, each device isolation region having a width taken from the range of values of 0.1 to 2.5 μm, wherein said grooves are formed before formation of the thermal oxide film,

wherein a width of each of the circuit regions is set such that a ratio of the width of each occurrence of a circuit forming region to the width of an adjacent device isolation region having a depth greater than 6 nm is at least 2 and not greater than 50, whereby the semiconductor device will be substantially free of dislocations which would otherwise be likely to occur, based on the depth of the grooves exceeding 6 nm, at portions of the main surface of the substrate located adjacent mask ends of a mask used to form the grooves.

Claim 21 (New): In a semiconductor device in which different circuit forming regions are electrically isolated from each other via isolation regions in the form of thermal oxide film formations, the improvement comprising:

a plurality of circuit forming regions provided at a main surface of said semiconductor substrate, respectively; and

device isolation regions provided as grooves, at least one of said grooves having a depth, extending inwardly from said main surface, greater than 6 nm and a thermal oxide film formed in said groove for isolating said circuit forming regions from one another, each device isolation region having a width taken from the range of values of 0.1 to 2.5 μm, wherein the grooves are formed before formation of the thermal oxide film,

wherein a width of each of the circuit forming regions is set such that a ratio of the width of each occurrence of a circuit forming region to the width of an adjacent device isolation region having a depth greater than 6 nm is at least 2 and not greater than 50, whereby the semiconductor device will be substantially free of dislocations which would otherwise be likely to occur, based on the depth of the grooves exceeding 6 nm, at portions of the main surface of the substrate located adjacent mask ends of a mask used to form the grooves.

Claim 22 (New): A semiconductor device according to claim 20, wherein said grooves have a depth of less than 50 nm.

Claim 23 (New): A semiconductor device according to claim 21, wherein said grooves have a depth of less than 50 nm.

Claim 24 (New): A semiconductor device according to claim 14, wherein each of said grooves is located a distance of 4-10 μm from an adjacent one of said circuit forming regions.

Claim 25 (New): A semiconductor device according to claim 16, wherein each of said grooves is located a distance of 4-10 μm from an adjacent one of said circuit forming regions.

Claim 26 (New): A semiconductor device according to claim 18, wherein each of said grooves is located a distance of 4-10 μm from an adjacent one of the circuit regions.

Claim 27 (New): A semiconductor device according to claim 19, wherein each of said grooves is located a distance of 4-10 μm from an adjacent one of said circuit forming regions.

Claim 28 (New): A semiconductor device according to claim 20, wherein each of said grooves is located a distance of 4-10 μm from an adjacent one of said circuit forming regions.

Claim 29 (New): A semiconductor device according to claim 21, wherein each of said grooves is located a distance of 4-10 μm from an adjacent one of the circuit regions.